

Harmonic analysis of Input Current of Single-Phase PFC Buck Converter

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ABSTRACT: The firing angle control of thyristor full wave ac-dc converters to set the desired DC bus voltage in Uninterruptible Power Supply (UPS) systems have drawbacks of pulsating input current, high harmonic content, low pf, low efficiency and large size of inductors and filters. International standards impose several constraints concerning the electric power quality and harmonic content of the line current in the equipment below some assigned limits. Hence there is a need to reduce the line current harmonics so as to improve the power factor of the system. In many applications, this distortion can be made acceptable with adequate line-current THD and PF performance. This paper proposes a PFC buck converter in UPS to set desired DC bus voltage which satisfies the EN61000-3-2 standards. The analysis of harmonic content and observed line voltage and current waveforms of hardware implemented are presented in this paper.

KEYWORDS: ac-dc converters, harmonic reduction, power factor correction (PFC), Total Harmonic Distortion (THD)

1. Introduction

The drive toward improving PF was initially mandated by European standard EN61000-3-2 [1] in an effort to reduce the harmonic content of the current flowing in the distribution network. More recently ENERGY STAR and European Commission initiatives have started to add PF requirements alongside efficiency specifications. For example, ENERGY STAR EPS 2.0 for external AC power supplies (such as adapters) now requires a minimum PF of 0.9 at full load at 115 VAC for power supplies with input power in the range of 100 W to 250 W. Power supplies for computing and consumer applications have and always will be severely cost-challenged, requiring cost-effective solutions to deliver both improved PF and efficiency, ability to operate across universal AC-mains voltage range efficiently and cost-effectively, without power derating, high-efficiency operation at light loading [1]. Solid state ac-dc conversion is used in adjustable speed drives, switch mode power supplies (SMPS), uninterrupted power supplies (UPS), solar PV, battery chargers, power supplies for telecommunication systems, test equipments etc. Power factor correction (PFC) is necessary for ac-to-dc converters in order to comply with the requirements of international standards, such as IEC 61000-3-2 and IEEE-519[2]. PFC can reduce the harmonics in the line current, increase the efficiency and capacity of power systems. The Active Power Factor Correction (APFC) is a method to improve the power factor near to unity, reduces harmonics distortion noticeably and automatically corrects the distorted line current. PFC draws more power from the mains when the level of the mains voltage is high and less power when it is low, which results in reduction of the harmonics in the drawn current[3].

Simple thyristor control circuit is shown in fig (1). In UPS systems internal DC bus voltage is controlled by adjusting thyristor/SCR firing angle in thyristor bridge rectifier as shown in fig(2). Traditional thyristors ac-dc converters draws pulsed current from the utility line when the thyristor is on. But percentage total harmonics distortion (THD%) increases with increase in firing angle. THD distortion is around 25% for 45° firing angle to 179% for 150° firing angle.[4] It is clear that for light or minimum loads when the firing angle is maximum there is a maximum distortion. Also there is an inherent “cross-over” distortion in the AC line current when the buck PFC stage is reverse biased. But in many applications, this distortion can be made acceptable with adequate line-current THD and PF performance[1]. Switching devices such as MOSFETs and IGBTs, is a result of advances in power semiconductor devices[7].

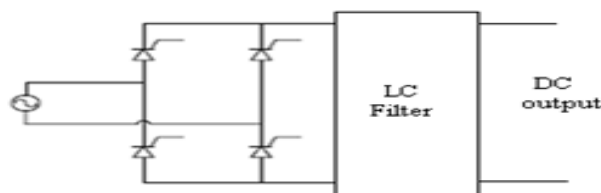


Fig1: Simplified Thyristor Control Circuit

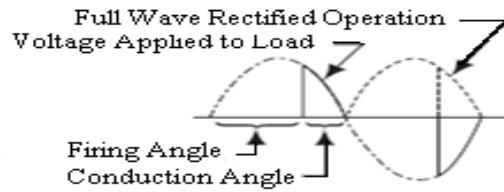


Fig2: Full wave bridge Thyristor firing in UPS AC-DC Converters

2. Harmonic Distortion and PF

Assuming an ideal sinusoidal input voltage source but when the current waveform is not an ideal sinusoidal then power factor can be expressed as the product of the distortion factor and the displacement factor (Fig.3). The distortion factor K_d , is the ratio of the fundamental root mean- square (RMS) current (I_{rms}) to the total RMS current (I_{rms}).

$$K_d = I_{rms(1)} / I_{rms}$$

The displacement factor $k\theta$ is the cosine of the displacement angle (ϕ) between the fundamental input current and the input voltage.

$$K_\theta = \cos \phi$$

For sinusoidal voltage and nonsinusoidal current, equation can be expressed as:

$$PF = \frac{V_{rms} I_{1,rms} \cos \phi}{V_{rms} \times I_{rms}} = \frac{I_{1,rms}}{I_{rms}} \cos \phi = K_d \cos \phi$$

$$PF = K_d K_\theta$$

In this case, the power factor depends on both harmonic content and displacement factor. The displacement factor $k\theta$ can be made unity with a capacitor or inductor, but making the distortion factor K_d unity is more difficult. In addition, the harmonic currents generated by the converter in the power source affects other equipment.

From the power factor triangle it is seen that by reducing the distortion angle θ i.e. by reducing current harmonics we can improve power factor. The total harmonic distortion (THD) is given by

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1}$$

where V_n is n^{th} harmonic amplitude and

V_1 is fundamental

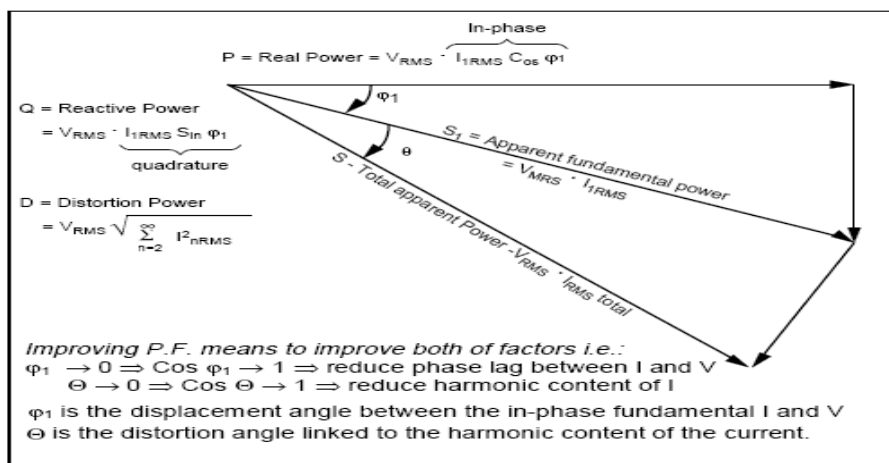


Fig.3: Harmonic distortion and Power factor triangle

Major two power factor correction techniques are Active PFC(APFC) and Passive PFC(PPFC). A passive PFC rarely achieves low Total Harmonic Distortion (THD). Also, the passive elements are normally bulky and heavy. Active PFC offers better THD and is significantly smaller and lighter than a passive PFC circuit. The active methods of PFC, which involve the shaping of the line current, using switching devices such as MOSFETs and IGBTs, is a result of advances in power semiconductor devices.

3. Buck PFC Overview

The basic circuit of the buck PFC power stage is shown in Fig. 4. This is a conventional buck (step-down) converter connected to an AC source and bridge rectifier. It is a voltage step down and current step up converter.

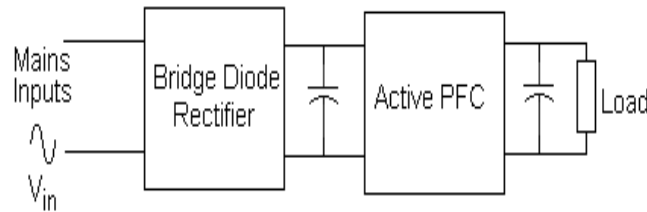


Figure 4: Block diagram of a rectifier with APFC

The output voltage for buck converter is given by

$$V_o = D * V_{in};$$

$$\text{Duty cycle } D = V_o / V_{in}.$$

4. Proposed Buck Converter

The proposed APFC buck converter uses IC 3525 as PWM. The control circuit diagram is given in fig(6). The output error voltage from op amp1 is used to control the required output dc voltage. The load current is set to required value by using error output of the proportional integral controller. The sensed load current is dual amplified and given to integrator summer inverting pin of op amp4 same as voltage control loop. Reference voltage of input line rectified at the 12-0-12 transformer as shown in circuit diagram is used to start the PWM pulses at the starting of each cycle to keep the current in phase with input line voltage. Soft start circuit provides smooth start of PWM pulses at the starting of the converter to increase the output voltage from zero to set value in a slow and smoothly manner. The error voltages from op amp1 and opamp4 which is applied at 3525 pin 9 have combine effect on PWM pulse width. The switching frequency used in this converter is 10 kHz. The Mitsubishi M57962L IGBT driver is used to drive the Mitsubishi IGBT. (TYPE CM100DU-12H). This converter can be used for higher load current ratings (up to 60 to70 A) by using suitable external IGBT and other power circuit components shown in fig.5 . The block diagram of IGBT driver is as shown fig.7 . The actual hardware system is shown in fig.8.

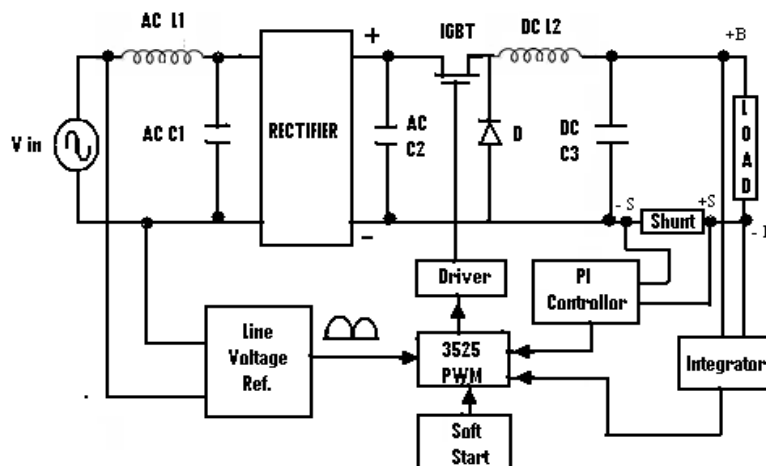


Fig5: Power Circuit and control circuit block diagram

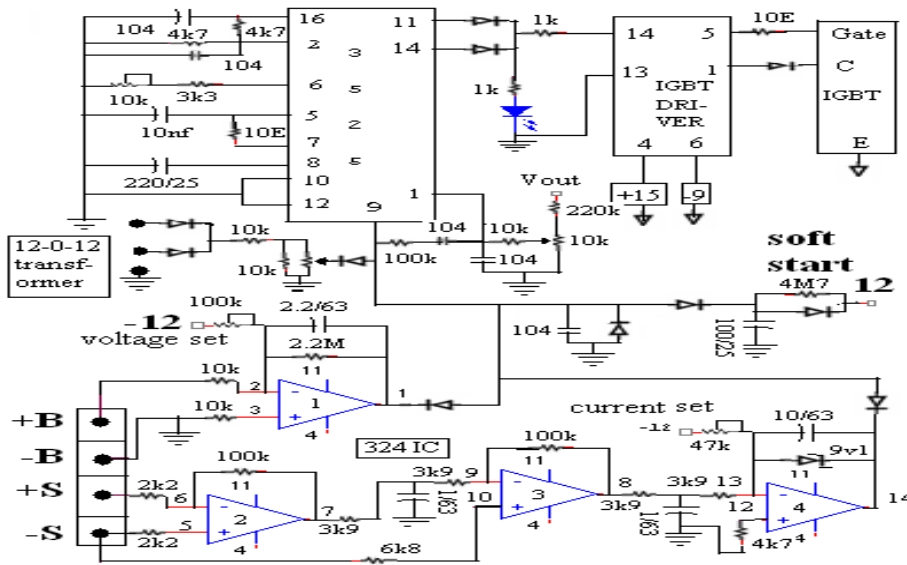


Fig6: Circuit diagram of Proposed Buck PFC Converter

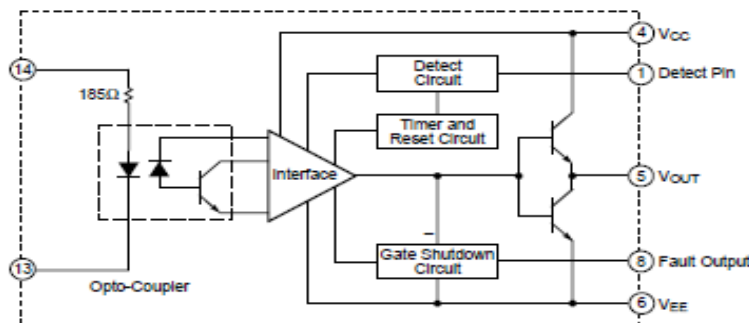


Fig 7. Block diagram of IGBT driver 57962

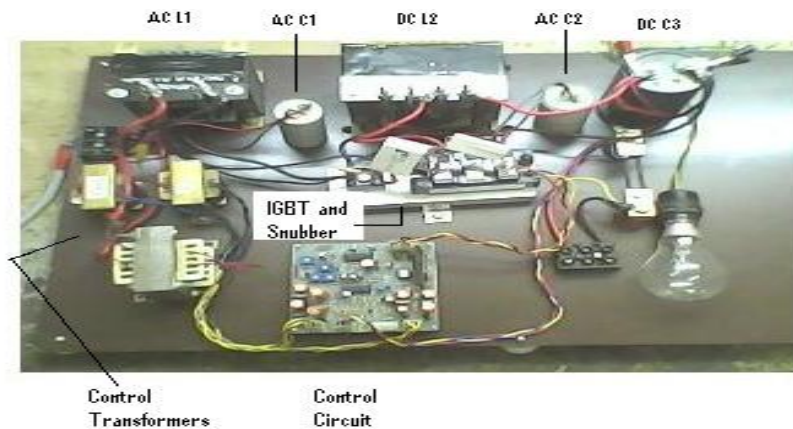


Fig 8. Hardware System of PFC converter

5. Results and Discussions

The results carried out with the circuit which is tested at various load conditions upto 1000W. Fig9 (a) shows voltage and current waveforms with proposed PFC scheme at the load of 270 Watt(1/4th load) and fig9(b) shows at 900Watt(full load). Fig 10(a) and 10(b) are the harmonic analysis results for 270W and 900W load respectively. harmonic analysis results are carried out using digital storage oscilloscope (FFT math function). In harmonic analysis results it is observed that fundamental component is dominant where as all other frequency components are comparatively suppressed. Fig(11) shows the input harmonics as compared with fundamental of proposed system along with limits according to EN 61000-3-2. In proposed buck converter the distortion is reduced appreciably. THD is 33.08% for 270W(1/4th load) and 34.13% for 900W (full load). Table I shows power factor results for various loads.

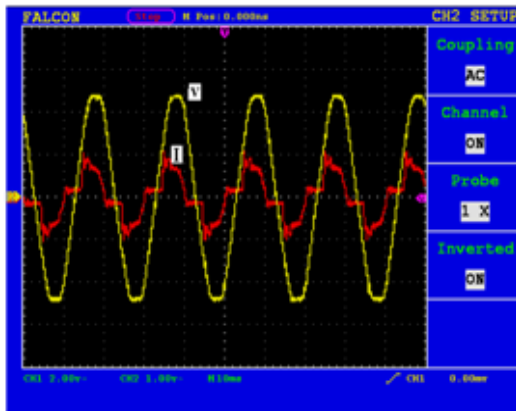


Fig9(a):Voltage &Current waveforms for 270W load

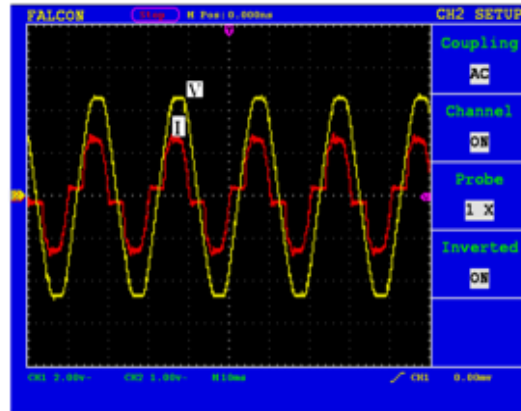


Fig9(b):Voltage & Current waveforms for 900W load



Fig10(a):-Harmonic analysis for 270W load

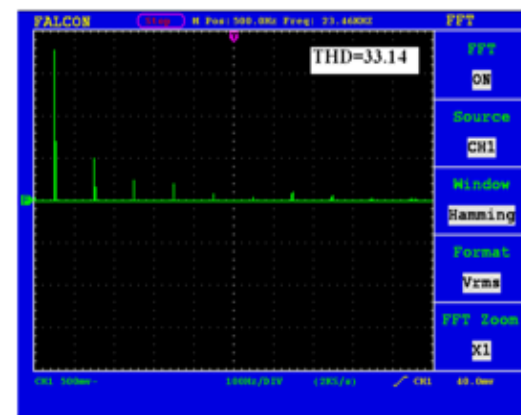


Fig10(b):-Harmonic analysis for 900W load

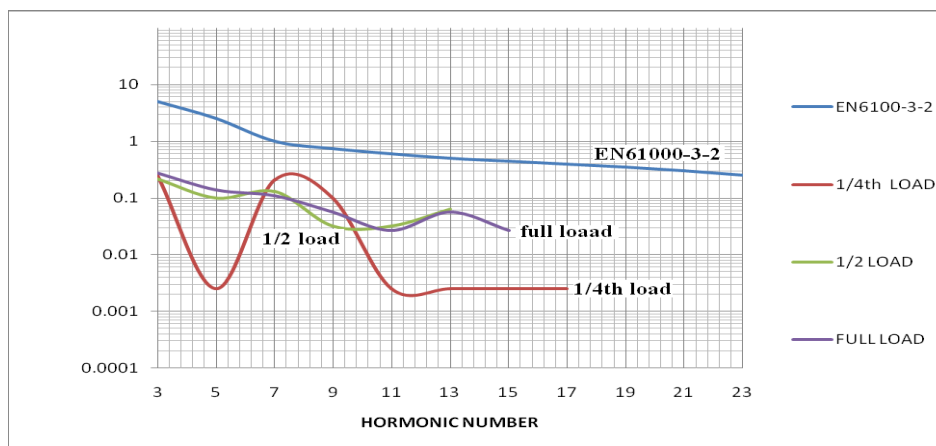


Fig11:Input characteristics with different loads

Table 1 Power Factor Results

O/P Load (W)	I/P Volt (V)	I/P Amp (A)	O/P Volt (V)	O/P Amp (A)	PF
54	242	0.4	135	0.4	0.675
135	242	0.8	135	1.0	0.779
270	242	1.4	135	2.0	0.864
473	241	2.2	135	3.5	0.916
904	240	3.9	135	6.7	0.954

6. Conclusions

The circuit is tested upto 1000W load and 135V output. Results shows that the THD is well within the EN61000-3-2 standard limits from 1/4th load to full load. Power factor varies from 0.864 to 0.954 for 1/4th load to full load. The output voltage can be widely controlled from 80V to 200V by selecting suitable power components. The converter is applicable in UPS dc bus, battery chargers, variable speed control of dc motors and similar applications.

7. Acknowledgement

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